NVM Express Technical Errata

Errata ID	**005**
Change Date	**9/23/2013**
Affected Spec Ver.	**NVM Express 1.0 and 1.1**
Corrected Spec Ver.	

Submission info

Name	Company	Date
John Carroll	Intel	4/17/2013
Ken Okin	Virident	4/17/2013
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Dave Landsman	SanDisk	4/17/2013
Jim Hatfield	Seagate	5/14/2013

Clarify the meaning of “secure erase”.

Clarified timeout value to be the time after enable rather than power on.

Clarified SMART global log page and added recommendation of what to do when specific log page is requested but not supported.

Added requirement for CC.MPS modification only while EN=0.

Various editorial changes.

Description of the specification technical flaw:

Modify a portion of section 4.8 as shown below:

A command is submitted when a Submission Queue Tail Doorbell write moves the Submission Queue Tail Pointer past the corresponding Submission Queue entry. The controller transfers submitted commands to the controller's local memory for subsequent processing using a vendor specific algorithm.
A command is being processed when the controller and/or namespace state is being accessed or modified by the command (e.g., a Feature setting is being accessed or modified or a logical block is being accessed or modified).
A command is completed when a Completion Queue entry for the command has been posted to the corresponding Completion Queue. Upon completion, all controller state and/or namespace state modifications made by that command are globally visible to all subsequently submitted commands.

Modify a portion of Figure 62 in section 5.8 as shown below:

Figure 62: Firmware Image Download – PRP Entry 2

Bit	Description
63:00	**PRP Entry 2 (PRP2):** This field contains the second PRP entry. If the data transfer is satisfied with PRP Entry 1, then this field is reserved. If the data transfer may be ~~satisifed~~ satisfied with two PRP entries total, then this entry specifies the location where data should be transferred from. If the data transfer requires more than two PRP entries, then this field contains a pointer to a PRP List.

Modify a portion of Figure 125 in section 6.5 as shown below:

Figure 125: Compare – PRP Entries or SGL Entry 1

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>127:00</td><td>If CDW0[15] is cleared to '0', then the definition of this field is:
<table>
<tr><td>127:64</td><td>PRP Entry 2 (PRP2): This field contains the second PRP entry. If the data to compare is satisfied with PRP Entry 1, then this field is reserved. If the data to compare may be ~~satisifed~~ satisfied with two PRP entries total, then this entry specifies the location that should be used for comparison. If the data transfer requires more than two PRP entries, then this field includes a pointer to a PRP List.</td></tr>
<tr><td>63:00</td><td>PRP Entry 1 (PRP1): This field contains the first PRP entry, indicating the location of data that should be used for comparison.</td></tr>
</table>
If CDW0[15] is set to '1', then the definition of this field is:
<table>
<tr><td>127:00</td><td>SGL Entry 1 (SGL1): This field contains the first SGL segment for the command, indicating the location of data that should be used for comparison.</td></tr>
</table>
</td></tr>
</table>

Modify a portion of Figure 138 in section 6.8 as shown below:

Figure 138: Read – PRP Entries or SGL Entry 1

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>127:00</td><td>If CDW0[15] is cleared to ‘0’, then the definition of this field is:

<table><tr><td>127:64</td><td>PRP Entry 2 (PRP2): This field contains the second PRP entry. If the data transfer is satisfied with PRP Entry 1, then this field is reserved. If the data transfer may be ~~satisifed~~ satisfied with two PRP entries total, then this entry specifies the location where data should be transferred to. If the data transfer requires more than two PRP entries, then this field includes a pointer to a PRP List.</td></tr><tr><td>63:00</td><td>PRP Entry 1 (PRP1): This field contains the first PRP entry, indicating the location where data should be transferred to.</td></tr></table>
If CDW0[15] is set to ‘1’, then the definition of this field is:

<table><tr><td>127:00</td><td>SGL Entry 1 (SGL1): This field contains the first SGL segment for the command, indicating the location where data should be transferred to.</td></tr></table></td></tr>
</table>

Modify a portion of Figure 160 in section 6.13 as shown below:

Figure 160: Write – PRP Entries ~~of~~ or SGL Entry 1

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>127:00</td><td>If CDW0[15] is cleared to ‘0’, then the definition of this field is:

<table><tr><td>127:64</td><td>PRP Entry 2 (PRP2): This field contains the second PRP entry. If the data transfer is satisfied with PRP Entry 1, then this field is reserved. If the data transfer may be ~~atisifed~~ satisfied with two PRP entries total, then this entry specifies the location where data should be transferred from. If the data transfer requires more than two PRP entries, then this field includes a pointer to a PRP List.</td></tr><tr><td>63:00</td><td>PRP Entry 1 (PRP1): This field contains the first PRP entry, indicating the location of data that should be transferred from.</td></tr></table>
If CDW0[15] is set to ‘1’, then the definition of this field is:

<table><tr><td>127:00</td><td>SGL Entry 1 (SGL1): This field contains the first SGL segment for the command, indicating the location of data that should be transferred from.</td></tr></table></td></tr>
</table>

Modify a portion of section 3.1.1 as shown below:

31:24	RO	Impl Spec	**Timeout (TO):** This is the worst case time that host software shall wait for ~~the controller to become ready (CSTS.RDY set to ‘1’) after a power-on or reset (section 7.3).~~ CSTS.RDY to transition from: a) ‘0’ to ‘1’ after CC.EN transitions from ‘0’ to ‘1’; or b) ‘1’ to ‘0’ after CC.EN transitions from ‘1’ to ‘0’. <INSERT BLANK LINE> This worst case time may be experienced after ~~an unclean shutdown~~ events such as an abrupt shutdown or activation of a new firmware image; typical times are expected to be much shorter. This field is in 500 millisecond units.

Modify a portion of Figure 82 in section 5.11 as shown below:

Figure 82: Identify – Identify Controller Data Structure

Admin Command Set Attributes & Optional Controller Capabilities		
…		
521:520	M	**Optional NVM Command Support (ONCS):** This field indicates the optional NVM commands and features supported by the controller. Refer to section 6. Bits 15:6 are reserved. Bit 5 if set to '1' then the controller supports reservations. If cleared to '0' then the controller does not support reservations. If the controller supports reservations, then it shall support the following commands associated with reservations: Reservation Report, Reservation Register, Reservation Acquire, and Reservation Release. Refer to section 8.8 for additional requirements. Bit 4 if set to '1' then the controller supports the Save field in the Set Features command and the Select field in the Get Features command. If cleared to '0' then the controller does not support the Save field in the Set Features command and the Select field in the Get Features command. Bit 3 if set to '1' then the controller supports the Write Zeroes command. If cleared to '0' then the controller does not support the Write Zeroes command. Bit 2 if set to '1' then the controller supports the Dataset Management command. If cleared to '0' then the controller does not support the Dataset Management command. Bit 1 if set to '1' then the controller supports the Write Uncorrectable command. If cleared to '0' then the controller does not support the Write Uncorrectable command. Bit 0 if set to '1' then the controller supports the Compare command. If cleared to '0' then the controller does not support the Compare command.
…		
524	M	**Format NVM Attributes (FNA):** This field indicates attributes for the Format NVM command. Bits 7:3 are reserved. Bit 2 indicates whether cryptographic erase is supported as part of the secure erase functionality. If set to '1', then cryptographic erase is supported. If cleared to '0', then cryptographic erase is not supported. Bit 1 indicates whether ~~secure~~ cryptographic erase and user data erase functionality ~~applies~~ apply to all namespaces or ~~is~~ are specific to a particular namespace. If set to'1', then a ~~secure~~ cryptographic erase of a particular namespace as part of a format results in a ~~secure~~ cryptographic erase of all namespaces, and a user data erase of a particular namespace as part of a format results in a user data erase of all namespaces. If cleared to '0', then a ~~secure~~ cryptographic erase or user data erase as part of a format is performed on a per namespace basis. Bit 0 indicates whether the format operation applies to all namespaces or is specific to a particular namespace. If set to '1', then all namespaces shall be configured with the same attributes and a format of any namespace results in a format of all namespaces. If cleared to '0', then the controller supports format on a per namespace basis.

Modify a portion of Figure 82 in section 5.11 as shown below:

Figure 82: Identify – Identify Controller Data Structure

261	M	**Log Page Attributes (LPA):** This field indicates optional attributes for log pages that are accessed via the Get Log Page command. Bits 7:1 are reserved. Bit 0 if set to '1' then the controller supports the SMART / Health information log page on a per namespace basis. If cleared to '0' then the controller does not support the SMART / Health information log page on a per namespace basis~~; the log page returned is global for all namespaces~~.

Modify a portion of section 5.10.1.2 as shown below:

This log page is used to provide SMART and general health information. The information provided is over the life of the controller and is retained across power cycles. The log page shall be supported on a global basis. To request the global log page, the namespace specified is FFFFFFFFh. The log page may also be supported on a per namespace basis, as indicated in the Identify Controller data structure in Figure 82. ~~To request the global log page, the namespace specified is FFFFFFFFh.~~ If the log page is not supported on a per namespace basis, specifying any namespace other than FFFFFFFFh should abort the command with status Invalid Field in Command.

Modify a portion of section 3.1.5 as shown below:

10:07	RW	0h	**Memory Page Size (MPS):** This field indicates the host memory page size. The memory page size is (2 ^ (12 + MPS)). Thus, the minimum host memory page size is 4KB and the maximum host memory page size is 128MB. The value set by host software shall be a supported value as indicated by the CAP.MPSMAX and CAP.MPSMIN fields. This field describes the value used for PRP entry size. This field shall only be modified when EN is cleared to '0'.

Modify a portion of section 7.7 as shown below:

If bit 4 is set to '1' in the Optional NVM Command Support field of the Identify Controller Data structure in Figure ~~65~~ 82 then for each Feature, there are three settings: default, saveable, and current. If bit 4 is cleared to '0' in the Optional NVM Command Support field of the Identify Controller Data structure in Figure ~~65~~ 82 then the controller only supports a current and default value for each Feature. In this case, the current value may be persistent across power states based on the information specified in Figure 89 and Figure 90.

Disposition log

4/17/2013	Erratum captured.
4/24/2013	Added requirement for CC.MPS modification only while EN=0. Added recommendation of what to do when specific log page is requested but not supported. Clarified CRC value for deallocated LBA's. Editorial changes.
5/3/2013	Removed clarification in Figure 111 on format and secure erase that will be covered in a technical proposal. Approved at Workgroup call for 30-day review.
5/14/2013	Edited the CC.TO (Timeout) language. Removed deallocate change as not needed.
5/14/2013	Editorial change to the FNA wording.
5/16/2013	Clarified CC.TO applies for firmware activation as a worst case timeout.
6/19/2013	Erratum ratified.
9/23/2013	Removed Version register change as the edit was incorrect.